HW#6

CSc 137, Singh

( 25Points)

For problems 6.1 through 6.3: Suppose the propagation delay of an 8-bit adder is 0.8ns, adder/subtractor is 1.1ns, 2-to-1 mux is 0.3ns, and 4-to-1 mux is 0.6ns. Also, assume register setup time (), clock-to-q (), and clock-skew () are all 0.05ns. (15 points)

* 1. Calculate the required maximum clock frequency for each of the following data paths:

1. Single-cycle data path in Fig. 6.2.
2. Multi-cycle data path in Fig. 6.3.
3. Pipelined data path in Fig. 6.4.
   1. Estimate the speedup between the following data paths when generating N = 1000 quantities *Ai + Bi + Ci ± Di* for i = 0, 1, 2, …, 999. Ignore the data reading and writing delays. (10 points)
4. Problem 6.1a vs. 6.1c

Extra Credit: 10 points

1. Non-return-to-zero inverted (NRZI) is a data coding scheme used to communicate with USB devices. The output signal (z) of a NRZI generator transitions when the input bit (x) is 0 and remains at constant previous value (0 or 1) when the input bit is 1. That is, from right to left when the input to the NRZI generator is 0 0 0 0 0 0, its output from right to left will transition as 1 0 1 0 1 0. Its output for consecutive 1s at the input, however, will remain at the previous output value. For example, the NRZI generator outputs from right to left z: 0 0 0 0 0 1 0 1 1 1 1 0 1 0 1 1 for input X: 1 1 1 1 0 0 0 1 1 1 0 0 0 0 1 1 read from right to left. Likewise, for X = 0xCF0C, Z: 0xEFAE. Design the NRZI generator. Design the circuit for the NRZI (Hint: design a Mealy FSM). (5 points)